Energy-band alignment of HfO2/SiO2/SiC gate dielectric stack


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The band alignment of HfO2/SiO2/SiC gate dielectric stack has been investigated by x-ray photoelectron spectroscopy and electrical characterization. Two types of valence band offsets are observed in the stack layer; the smaller value of 1.5 eV corresponds to the HfO2/SiC band offset while the larger one of 2.2 eV is due to the interfacial SiO2/SiC. The barrier height is extracted to be 1.5 eV from the Schottky emission characteristics and is higher than the reported value for HfO2 on SiC without interfacial SiO2. Thus, presence of an interfacial SiO2 layer increases band offsets to reduce the leakage current characteristics. © 2008 American Institute of Physics

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Figures 2(a) and 2(b) show Hf 4f and Si 2p core-level spectra of HfO2 (~3 nm)/SiO2 (~4 nm)/SiC gate dielectric stack at the surface as well as in the interfacial layer (between 3 and 8 nm depth), respectively. The spectra show strong signatures of HfO2 at the surface, indicated by the additional high energy features containing the information of the interfacial oxide layer. It is known that the binding energy difference between the stoichiometric SiO2 and SiC is about 3.5 eV. However, in Fig. 2(b), the high energy peak is gradually shifted toward the SiC substrate peak across the interfacial layer. The lower Si 2p binding energy shifts (2.0–2.6 eV) from the SiC peak is due to the result of the silicate-like compound in the interfacial layer rather than a pure SiO2. As the substrate temperature during Hf deposition is low, the silicate may be formed during the oxidation of Hf at 650 °C.

Figure 3(a) shows the current versus gate voltage characteristics of the Al/HfO2 (~25 nm)/SiO2 (~6 nm)/SiC MOS capacitor at various temperatures under substrate electron injection. The experimental results at higher temperatures fit the Schottky emission theory very well, as shown in the inset of Fig. 3(b). The current vs. gate voltage characteristics of the Al/HfO2 (~25 nm)/SiO2 (~6 nm)/SiC and HfO2 (~25 nm)/SiC gate dielectrics.

FIG. 1. (Color online) (a) the valence band (VB) spectrum of 4H-SiC substrate. (b) The VB spectra of (i) bulk HfO2 (~25 nm), (ii) bulk SiO2, and (iii) HfO2 (~3 nm)/SiO2 (~4 nm)/SiC, respectively. Two valence band offsets of 1.5 and 2.2 eV are observed for HfO2/SiO2/SiC layer, as shown in the inset.
height, the band gap of the interfacial oxide layer is extracted to be 6.96 eV. It is interesting to note that the band gap of interfacial oxide layer is reduced from the actual value (~8.9 eV) of SiO2. This is due to the intermixing of HfO2 and SiO2 layers in the interface which is elucidated by XPS core level spectra as discussed earlier and this extracted band gap value is comparable to the reported value of Hf silicate.

In conclusion, the band alignment of HfO2/SiO2/SiC gate dielectric stack has been investigated using x-ray photoelectron spectroscopy and electrical characteristics. Two valence band maxima features are observed in the stack layer. The smaller band offset of 1.5 eV corresponds to the HfO2/SiC band offset while the larger one of 2.2 eV is due to the interfacial SiO2/SiC. The barrier height or conduction band offset is extracted to be 1.5 eV. Thus the growth of an initial SiO2 layer increases band offsets to reduce the leakage current characteristics which suggests that the HfO2/SiO2/SiC stack layer will be a potential gate dielectric for SiC-based MOS device applications. A further optimization to grow the dielectric stack with an abrupt interface is believed to improve the interface morphology and also the electrical properties. In particular, a strong attention should be given to minimization of the formation of the intermixing layer at the interface.

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